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10/568,279	02/15/2006	**Gordon John Allan**	51959-1 /slr	3290

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EXAMINER	
TRA, ANH QUAN	
ART UNIT	**PAPER NUMBER**
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/568,279	ALLAN, GORDON JOHN	
	Examiner	Art Unit	
	QUAN TRA	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,20-31 and 33-41* is/are rejected.

7)☒ Claim(s) *18, 19 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 7/21/08. A new ground of rejection is introduced.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-12, 17, 20-27, 30-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okajima (US 20060273840)

As to claim 1, Okajima's figure 16 shows a delay circuit but fails to show the pulse width of control signal CLK or a value of "N". It is seen as an obvious design preference to select any value for the pulse width (i.e. small value) or "N' (very high value) dependent upon a particular environment of use to ensure optimum performance. Thus, the modified Iwamoto's figure 5 shows a circuit comprising: a plurality of mixed-signal outputs (outputs of A1-An or B1-Bn); a first set of driving elements (A1-An) connected together in sequence each having a respective output connected to a respective one of the mixed-signal outputs; the first set of driving elements having a first driving element and having a last driving element; a second set of driving elements (B1-Bn) connected together in sequence each having a respective output connected to a respective one of the mixed signal outputs in an order opposite to an order of connection of the first set of driving elements to the mixed signal outputs, the second set of driving elements having a first driving element and a last driving element; wherein while in a first control state (when CLK is Ihigh) the first set of driving elements drives each of the mixed-signal outputs

towards a respective off state sequentially in a direction from the first driving element of the first set towards the last driving element of the first set such that any mixed-signal output that is driven only partially towards its respective off state maintains an analog value (if the output of any one of the inverters A1-An is not fully low (partially low) when inverters A1-An are at the high impedance states (tri-states), that output value is maintained and considered as the analog value); and wherein while in a second control state (when CLK is low) the second set of driving elements drives each. of the mixed-signal outputs towards a respective on state sequentially in a direction from the first driving element of the second set towards the last driving element of the second set such that any mixed-signal output that is driven only partially towards its respective on state maintains an analog value (when the inverters B1-Bn are at the high impedance states); wherein while in a third control state (between high and low) each mixed-signal value maintains its respective value.

As to claim 2, figure 16 shows two control inputs (outputs of I3 and I4) that define the first, second and third control states. :

As to claim 3, figure 16 shows that each driving element is a tri-state buffer (two inverters), and each of the on states are represented by a high voltage, and each of the off states are represented by a low voltage.

As to claim 4, figure 16 shows that each driving element is an inverter, and each of the on states alternate between being represented by a low voltage and a high voltage, and each of the on states alternate between being represented by a high voltage and a low voltage.

As to claim 5, figure 16 shows a logic on biasing circuit (transistors that receive CLK signals in inverter A1-An) that biases on voltage of any active high control input to an amount below logic high and/or biases any active low control input (at node between 33 and 34) to an amount above logic low.

As to claim 6, figure 16 shows a logic off biasing circuit (transistors receives CLK signals in inverters B1-Bn) that biases an off voltage of any active high control input to an amount above logic low and/or biases any active low control input to an amount below logic high.

As to claim 7, figure 16 shows each driving element is a single-transition driving element.

As to claim 8, tunable filter is well known in the art for reducing unwanted noise. It would have been obvious to one having ordinary skill the art add a tunable filter connected between the control input(s) and the driving elements for the purpose of reducing noise.

As to claim 9, tunable filter is well known in the art for reducing unwanted noise. It would have been obvious to one having ordinary skill the art add filter connected to each of the mixed-signal outputs for the purpose of reducing the outputs' noises.

As to claim 10, it is seen as an intended use to select the outputs of A1-An to drive any not shown circuit(s), which are considered as circuitry to dynamically determine a subset of the mixed signal outputs.

As to claim 11, the modified figure 16 show at least one additional filter (see the rejection of claims 8 and 9); circuitry (circuits that are drove by the outputs of A1-An) that dynamically connects the at least one additional filter to mixed- signal outputs that are outputting analog values.

As to claim 12, the modified figure 16 shows that the at least one filter has at least one dynamically adjustable filter characteristic.

As to claim 17, figure 16 shows steering logic (I1-I4) for directing signals received on the at least one control input to a subset of the driving elements that are generating analog values

As to claims 20-22, figure 16 is a delay circuit. One skilled in the art would have motivated to use the delay circuit figure 16 in a delay locked loop in order to take advantage of circuit figure 16's benefits, such as low noise and power consumption

Claims 23 and 24 recite similar limitations of claims above. Therefore they are rejected for the same reasons.

As to claim 25, figure 16 shows that the step of dynamically determining which of the set of mixed-signal outputs are outputting an analog value comprises: for each of at least one particular nixed-signal output, receiving at least one neighboring mixed-signal outputs; determining the mixed-signal output is analog if the neighboring mixed-signal output(s) are consistent with the particular mixed-signal output being analog value for a mixed-signal thermometer code (any code).

As to claim 26, figure 16 shows the step of dynamically connecting at least one additional filter to the mixed-signal outputs (see the rejection of claims 8 and 9) that are outputting analog values.

As to claim 27, figure 16 shows the step of maintaining (in the tri-state) a respective state for each of the mixed-signal outputs that are outputting analog values.

Claims 30-31 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

As to claim 33, figure 16 shows a circuit comprising: at least one control input (outputs if I3 and I4) defining at least a first control state and a second control state; a plurality of mixed-signal outputs (outputs of A1-An) each characterized by a respective on state (high), a respective off state (low), and a respective analog range (transition time between high and low); a set of circuit elements (A1-An and B1-Bn) connected to cause sequential transitions of any mixed- signal output that is in a respective off state or in the respective analog range towards a respective on state during the first control state, and to cause sequential transitions of any mixed-signal output that is in a respective on state or in the respective analog range towards a respective off state during the second control state.

As to claim 34, figure 16 shows show that the on states are all logic high and the off states are all logic low.

As to claim 35, figure 16 shows that the on states alternate between being logic high and logic low, and the off states alternate between being logic low and logic high.

As to claim 36, figure 16 show a method for dynamically determining if a particular output of a set of mixed-signal outputs representing a mixed signal code is outputting an analog value, the method comprising: receiving at least one neighboring mixed-signal outputs (by A1-An and B1-Bn); determining (generates out base on the value input) if the neighboring mixed-signal outputs are consistent with the particularity mixed-signal output being an analog value for the mixed-signal code (any code).

As to claim 37, figure 16 shows that the mixed-signal code is a thermometer code (intended use).

As to claim 38, figure 16 shows the step of dynamically connecting at least one additional capacitance or filter stage to the mixed-signal outputs that are outputting analog value (see the rejection of claims 8 and 9).

3. Claims 13 -16, 27-29, 39-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okajima (US 20060273840) in view of Matsuda et al. (USP 5761134).

As to claim 14, Okajima's figure 16 fails to show circuitry for maintaining an approximate state of the mixed-signal outputs. However, Matsuda's figure 5 shows a latch circuit 4 coupled to the output of tri-state inverter 2 in order to maintain an approximate state of its output. Therefore, it would have been obvious to one having ordinary skill in the art to add latch circuit to the output of each of Saeki et al.'s inverters for the purpose of maintaining the inverters' outputs when disabled.

As to claim 15, the modified figure 16 shows at least one state (the added latch) maintaining element for maintaining an approximate state of the mixed-signal outputs upon power down or idle modes of the circuit; circuitry (wire) to dynamically connect the at least one state maintaining element to the mixed-signal outputs determined to be outputting analog values.

As to claim 16, the modified figure 16 shows that the circuitry for maintaining the approximate state of the mixed signal-outputs which maintains a reduced number of states from which the entire approximate state can be deduced.

Claims 27-29 and 39 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

As to claim 40, the modified figure 16 shows a method for processing a set of mixed-signal outputs, each mixed signal output characterized by a digital state and an analog state, the method comprising: detecting (by the added latches, A1-An and B1-Bn) when a particular mixed-signal output has reached a digital state; upon detecting that a particular mixed-signal output has reached the digital state, securing the particular mixed-signal output to an appropriate reference.

As to claim 41, the modified Okajima's figure 16 shows that the set of mixed-signal outputs represent a mixed-signal code, and wherein detecting when a particular mixed-signal output has reached a digital state comprises: receiving at least one neighboring mixed-signal outputs (by the latches, A1-An and B1-Bn); determining if the neighboring mixed-signal outputs are consistent with the particular mixed-signal output being a digital state for the mixed-signal code (by generating outputs in response to the inverters' input).

Allowable Subject Matter

4. Claims 18, 19 and 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to QUAN TRA whose telephone number is (571)272-1755. The examiner can normally be reached on 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 571-272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/QUAN TRA/
Primary Examiner, Art Unit 2816